

FIG. 1

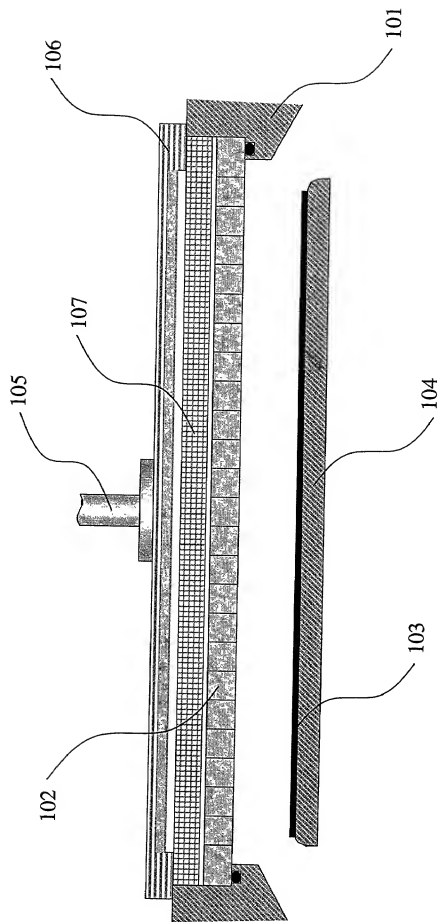


FIG. 2

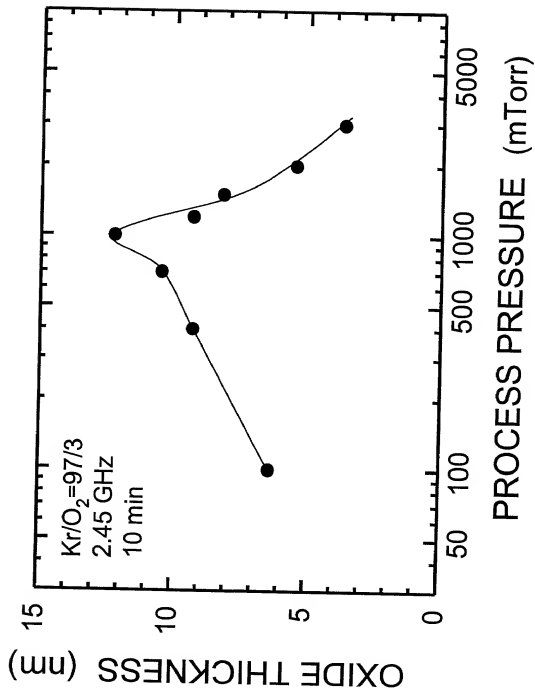


FIG. 3

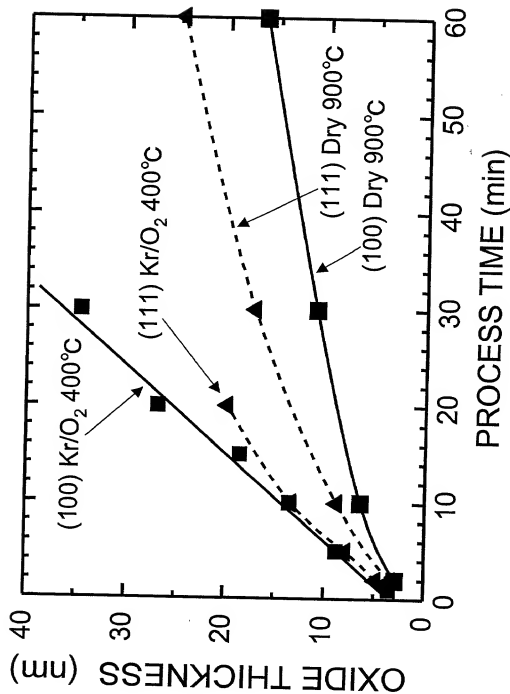


FIG. 4

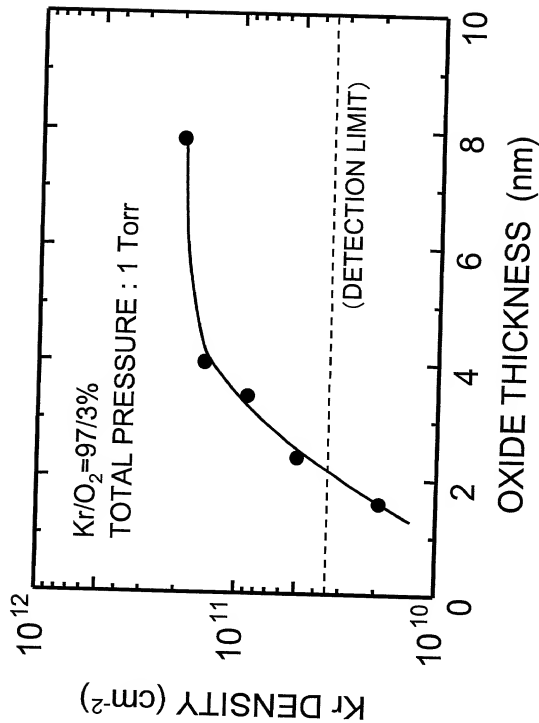


FIG. 5

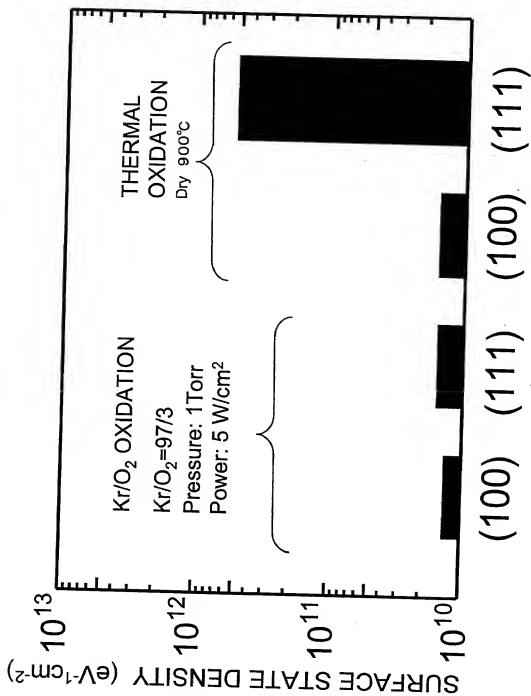


FIG. 6

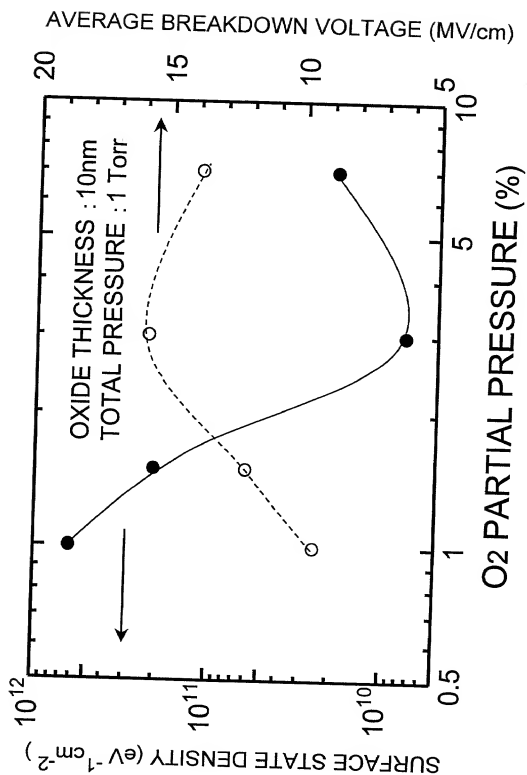


FIG. 7

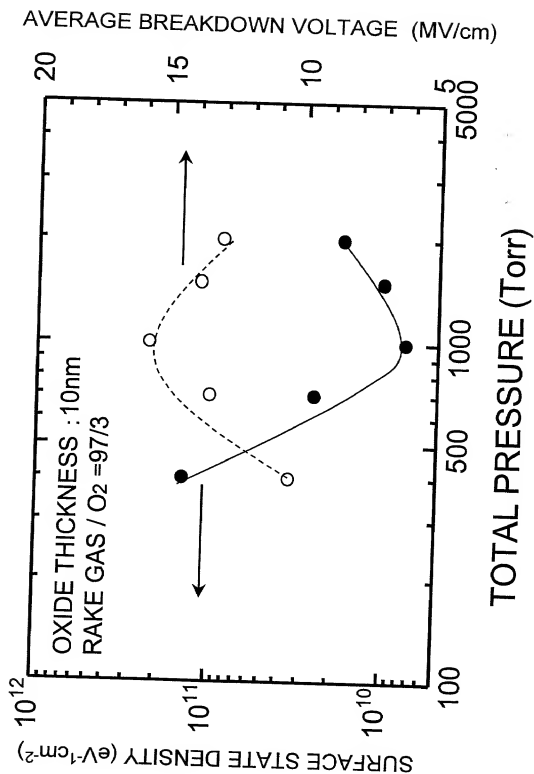


FIG. 8

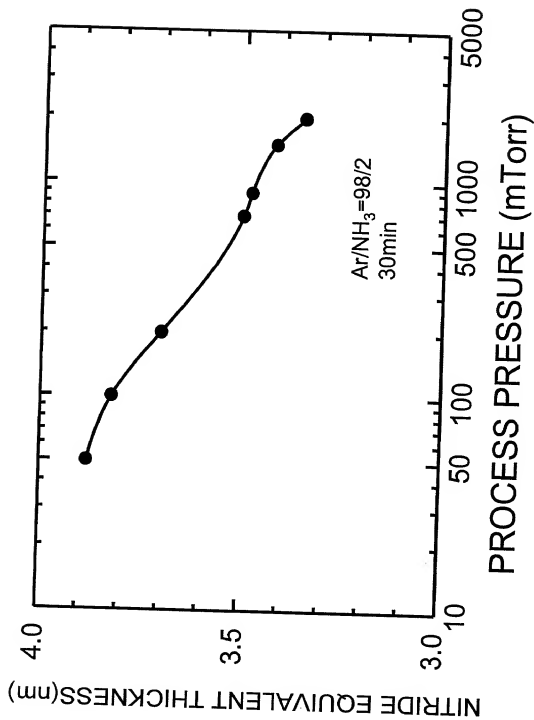
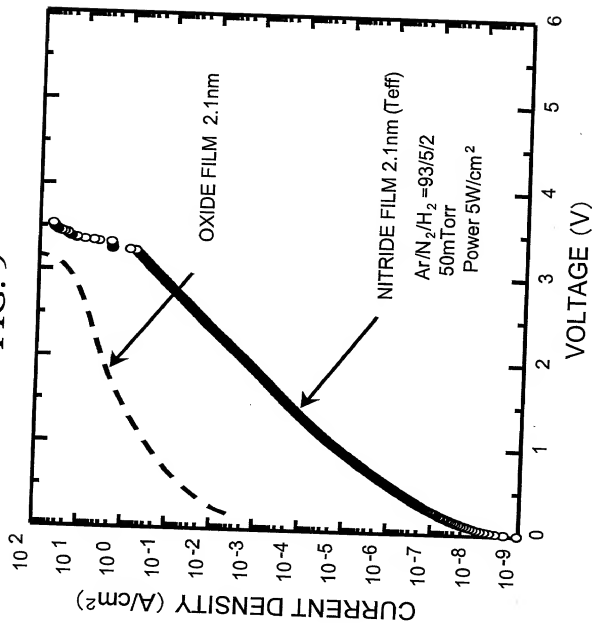




FIG. 9



12 { 12B 12A 11

(100) or (111) Si substrate

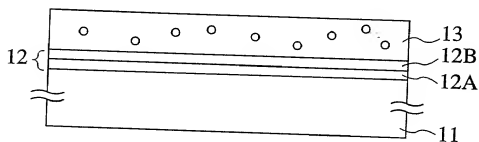


FIG. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 11 with a central region 11A and side regions 11B and 11D. A gate structure 12 is formed on top of region 11A, comprising gate electrodes 12A and 12B. A source/drain region 13A is formed on top of region 11B. A contact layer 14 is formed on top of region 11D, with contact electrodes 14A and 14B. A dimension  $L_g$  is indicated between the gate and contact regions.

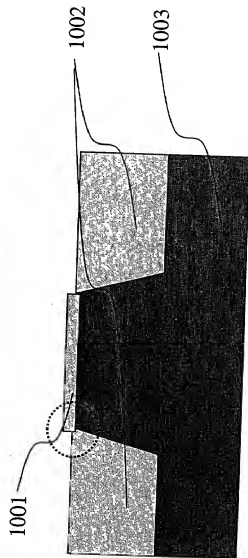


FIG. 11A

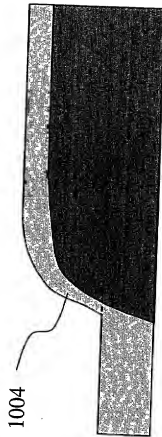


FIG. 11B

PRIOR ART

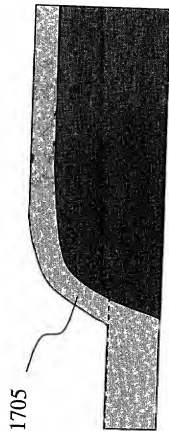


FIG. 11C

PRESENT INVENTION

FIG. 12

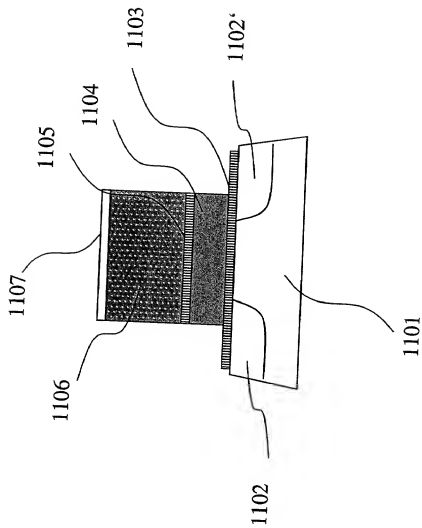


FIG. 13

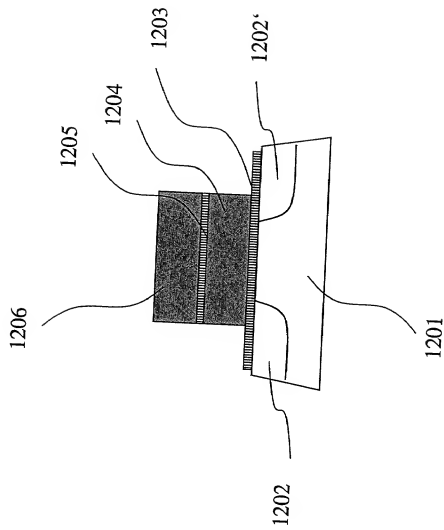


FIG. 14



FIG. 15

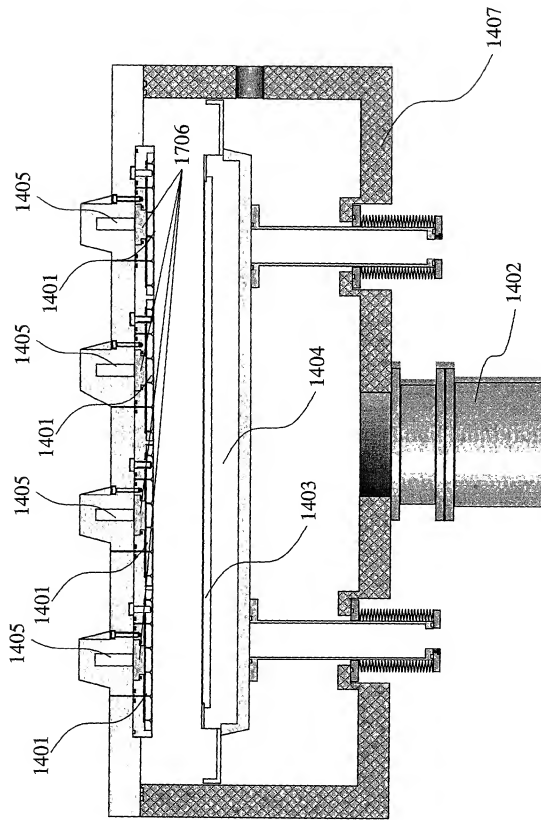


FIG. 16

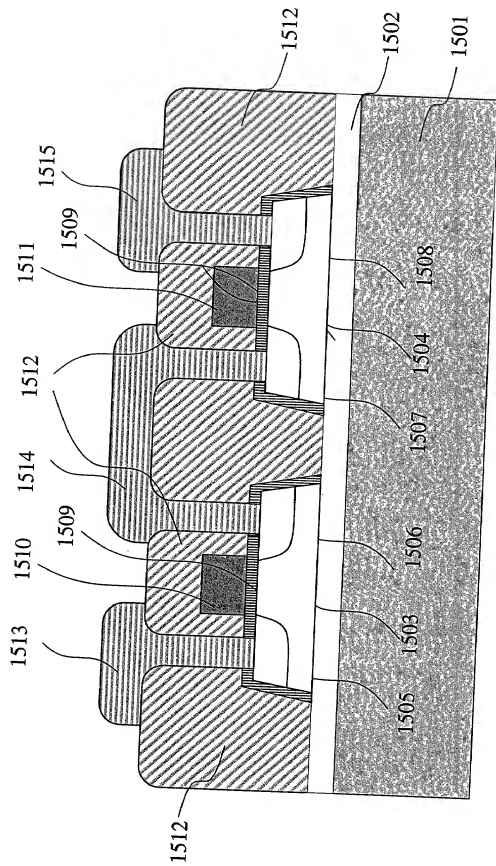




FIG. 17

